Features

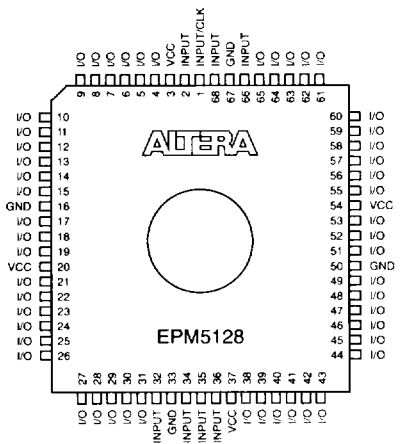
- High-density 128-macrocell general-purpose MAX 5000 EPLD
- 256 shareable expander product terms that allow over 32 product terms in a single macrocell
- High-speed multi-LAB architecture
  - t_{PD} as fast as 25 ns
  - Counter frequencies up to 50 MHz
  - Pipelined data rates up to 62.5 MHz
- Programmable I/O architecture allowing up to 60 inputs or 52 outputs
- Available in 68-pin windowed ceramic or plastic one-time-programmable (OTP) J-lead packages and in 68-pin windowed ceramic PGA packages

General Description

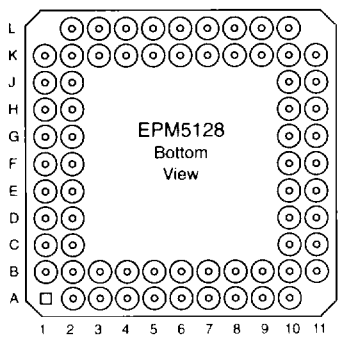
The Altera EPM5128 EPLD is a user-configurable, high-performance Multiple Array MatriX (MAX) 5000-family EPLD that provides a high-density replacement for 7400-series SSI and MSI TTL and CMOS logic. For example, a 74161 counter uses only 3% of the EPM5128 EPLD. The EPM5128 EPLD can replace over 60 TTL MSI and SSI components and integrate multiple 20- and 24-pin low-density PLDs. Figure 18 shows the J-lead and PGA package diagrams for the EPM5128 EPLD.

Figure 18. EPM5128 Package Pin-Out Diagrams

See Table 2 in this data sheet for PGA package pin-outs. Package outlines not drawn to scale.



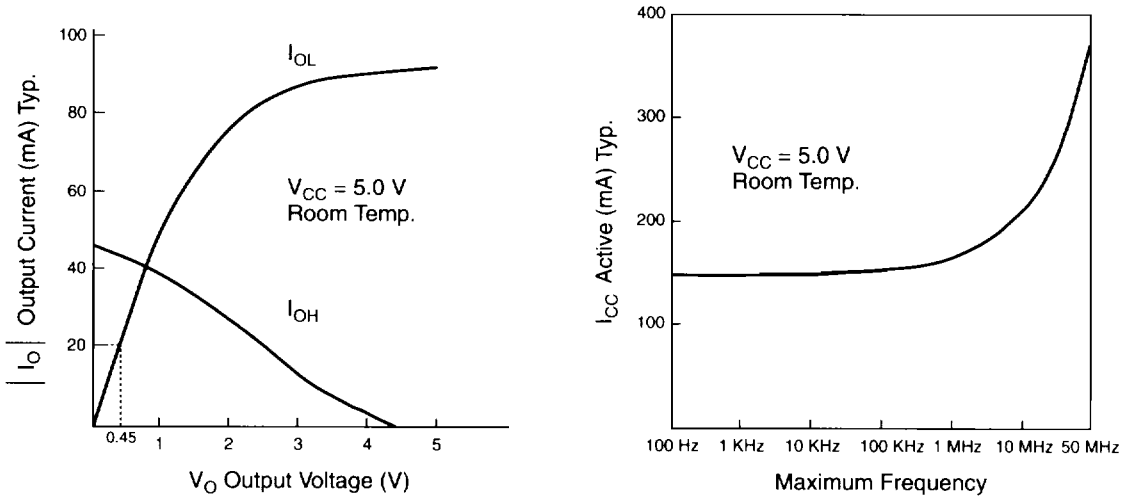
J-Lead



PGA

Figure 19 shows output drive characteristics of EPM5128 I/O pins and typical supply current versus frequency for the EPM5128 EPLD.

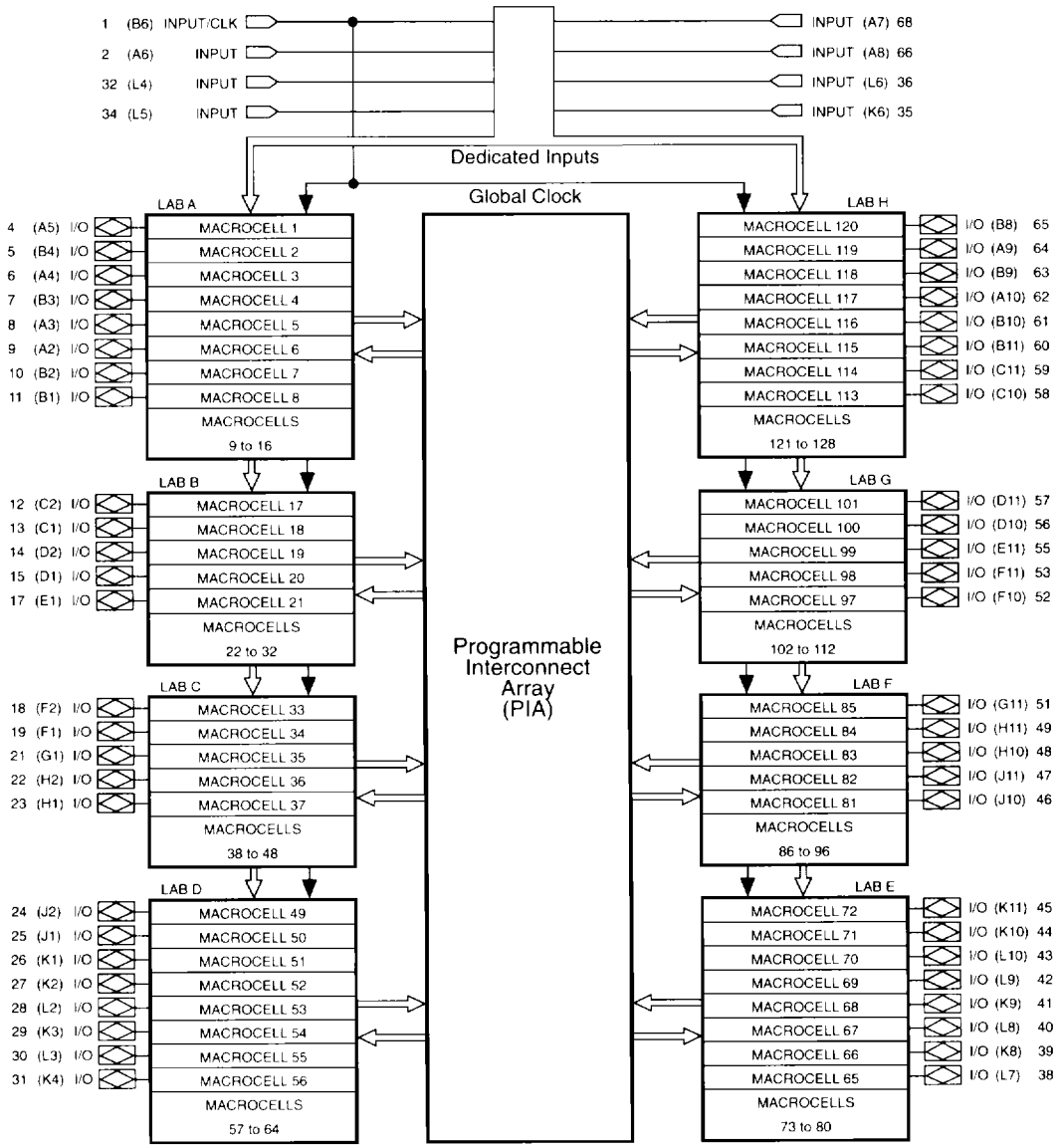
Figure 19. EPM5128 Output Drive Characteristics and I_{CC} vs. Frequency



The EPM5128 EPLD consists of 128 macrocells equally divided into 8 Logic Array Blocks (LABs) that each contain 16 macrocells (see Figure 20). Each LAB also contains 32 expander product terms. The EPM5128 EPLD has 8 dedicated input pins, one of which may be used as a global (synchronous) system clock. The EPM5128 device contains 52 I/O pins that can be configured for input, output, or bidirectional data flow. Four of the LABs have 8 I/O pins, and the other 4 have 5 I/O pins.

Figure 20. EPM5128 Block Diagram

Numbers in parentheses are for PGA packages.



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			500	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

See Note (2)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions

See Notes (2), (3), (4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND		150	225 (300)	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (5)*		155	250 (350)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *See Note (4)*

External Timing Parameters			EPM5128-1		EPM5128-2		EPM5128		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Unit
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	ns
t_{PD2}	I/O input to non-registered output			40		45		55	ns
t_{SU}	Global clock setup time		15		20		25		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		14		16		20	ns
t_{CH}	Global clock high time		8		10		12.5		ns
t_{CL}	Global clock low time		8		10		12.5		ns
t_{ASU}	Array clock setup time		5		6		8		ns
t_{AH}	Array clock hold time		6		8		10		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		25		30		35	ns
t_{ACH}	Array clock high time	*See Note (6)*	11		14		16		ns
t_{ACL}	Array clock low time		9		11		14		ns
t_{CNT}	Minimum global clock period			20		25		30	ns
f_{CNT}	Max. internal global clock frequency	*See Note (5)*	50		40		33.3		MHz
t_{ACNT}	Minimum array clock period			20		25		30	ns
f_{ACNT}	Max. internal array clock frequency	*See Note (5)*	50		40		33.3		MHz
f_{MAX}	Maximum clock frequency	*See Note (7)*	62.5		50		40		MHz

Internal Timing Parameters *See Note (8)*			EPM5128-1		EPM5128-2		EPM5128		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Unit
t_{IN}	Input pad and buffer delay			5		7		9	ns
t_{IO}	I/O input pad and buffer delay			6		6		9	ns
t_{EXP}	Expander array delay			12		14		20	ns
t_{LAD}	Logic array delay			12		14		16	ns
t_{LAC}	Logic control array delay			10		12		13	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5		5		6	ns
t_{ZX}	Output buffer enable delay			10		11		13	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		10		11		13	ns
t_{SU}	Register setup time		6		8		10		ns
t_{LATCH}	Flow-through latch delay			3		4		4	ns
t_{RD}	Register delay			1		2		2	ns
t_{COMB}	Combinatorial delay			3		4		4	ns
t_{H}	Register hold time		6		8		10		ns
t_{IC}	Array clock delay			14		16		18	ns
t_{ICS}	Global clock delay			2		2		3	ns
t_{FD}	Feedback delay			1		1		2	ns
t_{PRE}	Register preset time			5		6		7	ns
t_{CLR}	Register clear time			5		6		7	ns
t_{PIA}	Prog. Interconnect Array delay			14		16		20	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Numbers in parentheses are for military and industrial temperature-range versions.
(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(5) Measured with a device programmed as a 16-bit counter in each LAB.
(6) This parameter is measured with a positive-edge-triggered clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(7) The f_{MAX} values represent the maximum frequency for pipelined data.
(8) For information on internal timing parameters, refer to *Application Brief 75*.

Product Availability

Operating Temperature		Availability
Commercial	(0° C to 70° C)	EPM5128-1, EPM5128-2, EPM5128
Industrial	(–40° C to 85° C)	EPM5128
Military	(–55° C to 125° C)	EPM5128

Note: Only military-temperature-range EPLDs are listed above. MIL-STD-883-compliant product specifications are provided in Military Product Drawings (MPDs), available by calling Altera Marketing at (408) 984-2800. These MPDs should be used to prepare Source Control Drawings (SCDs). See *Military Products* in this data book.

Table 2 shows the pin-outs for the EPM5128 PGA package.

Table 2. EPM5128 PGA Pin-Outs

Pin	Function	Pin	Function	Pin	Function	Pin	Function
A2	I/O	B9	I/O	F10	I/O	K4	I/O
A3	I/O	B10	I/O	F11	I/O	K5	GND
A4	I/O	B11	I/O	G1	I/O	K6	INPUT
A5	I/O	C1	I/O	G2	VCC	K7	VCC
A6	INPUT	C2	I/O	G10	GND	K8	I/O
A7	INPUT	C10	I/O	G11	I/O	K9	I/O
A8	INPUT	C11	I/O	H1	I/O	K10	I/O
A9	I/O	D1	I/O	H2	I/O	K11	I/O
A10	I/O	D2	I/O	H10	I/O	L2	I/O
B1	I/O	D10	I/O	H11	I/O	L3	I/O
B2	I/O	D11	I/O	J1	I/O	L4	INPUT
B3	I/O	E1	I/O	J2	I/O	L5	INPUT
B4	I/O	E2	GND	J10	I/O	L6	INPUT
B5	VCC	E10	VCC	J11	I/O	L7	I/O
B6	INPUT/CLK	E11	I/O	K1	I/O	L8	I/O
B7	GND	F1	I/O	K2	I/O	L9	I/O
B8	I/O	F2	I/O	K3	I/O	L10	I/O